SoC HUB ONLINE WORKSHOP

MAKING OF SoCs

System-on-Chip design flow

Thursday 25 March 2021

SoC HUB

SoC HUB Speakers

- ***Timo Hämäläinen*** is a professor of Computer Engineering and the head of Computing Sciences at Tampere University. At SoC Hub he contributes to the ecosystem management, leads and supervises research projects and participates in SoC Hub ecosystem building.

- ***Antti Rautakoura*** works as an architect and project manager at SoC Hub as well as PhD researcher at Tampere University. He is specialised in SoC/ASIC verification and has also a strong industry background from Nokia Mobiles, Renesas Electronics and Nokia Networks.

- ***Suvi Lammi*** works as a coordinator at SoC Hub. She contributes to communications, marketing and events among other things.

SoC HUB Workshop Outline 25.3.2021

- ***9.00*** Opening and overview to SoC Hub
  Timo Hämäläinen
- ***9.10*** Quiz
  Suvi Lammi
- ***9.15*** Part I: SoC landscape and design flow
  Antti Rautakoura
- ***10.15*** Questions & Answers
- ***10.30*** SoC Hub update
  Timo Hämäläinen
- ***10.45*** Part II: Managing the project – Design, infrastructure, resources, schedule and costs
  Antti Rautakoura
- ***11.45*** Questions & Answers
- ***12.00*** Closing words
  Timo Hämäläinen
- ***12.15*** Workshop close

SoC HUB

Opening
Overview of SoC Hub

Timo Hämäläinen

SoC Hub Goals

- Bring together all stakeholders from applications to SoC experts to start new ecosystem
- Co-create SoC template and prototype chips
- Share the results, methodology and experiences for new research and products

SoC Hub template & chips

Fundamentals - SoC 2021

Boot CPU | IO | AI / ML | DSP | MCU | C2C (to FPGA)

"IoT capable"

22nm

Connectivity - SoC 2022

Boot CPU | IO | AI / ML | 1G ETH | DSP | MCU | Wireless connectivity | C2C

"Edge capable"

SoC Hub template for new products

SoC scaled up/down as needed

Full featured - SoC 2023

Boot CPU | IO | AI / ML | RISC-V high end CPU | 10G ETH | Security | DSP | MCU | Wireless connectivity | Video codec | DDR

"ML capable"

Boot Software | Firmware and drivers | Linux | Application SW

SoC Hub overall timeline

TODAY:

SoC Hub Events

Workshops/webinars, Hackathons, SoC Hub coffee

SoC Hub Sprints

SoC prototype 1

SoC prototype 2

SoC prototype 3

SoC Hub expertise

SoC Hub architecture template & IPs & methodology

2021 2022 2023 2024

Workshop objectives

- What is SoC design flow
  - What is different to SW design, FPGA design, general embedded systems design
  - What tools, infrastructure, supply chain is needed
  - What resources and skills are needed
  - Can it be agile like SW?
- What is SoC business
  - Who are the stakeholders
  - What is IPR
  - What does SoC cost

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Webinar quiz & feedback form

Suvi Lammi

SoC HUB Quiz

During the presentation

- Questions from the presentations – what do you think, evaluate the content from your point of view

Afterwards

- Feedback form via email – did you learn and did you like the seminar
- Your needs and goals for SoC design flow and management of the project?

Privacy: Participant contributions are collected for reporting summary information to public funding agency about the engagement and impact of the SoC Hub activities

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Part I: SoC design flow

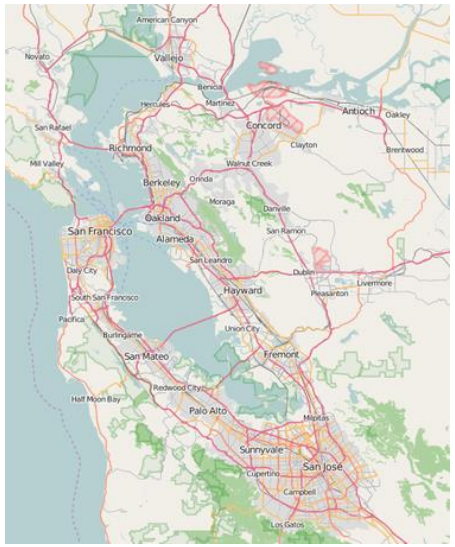
Antti Rautakoura

SoC HUB Agenda

Part I 60min +15 discussions

Introducing the landscape as base to understand the more detailed design flow

- IC Technology in short
- SoC terms and concepts
- SoC product examples
- Stakeholders around
- SoC design flow



Instead of

Part II 60min +15 discussions

Understanding the complexity, schedule and costs as tool to manage SoC projects

- Scale of complexity
- Scale of costs
- Example calculations about the costs

Instead of

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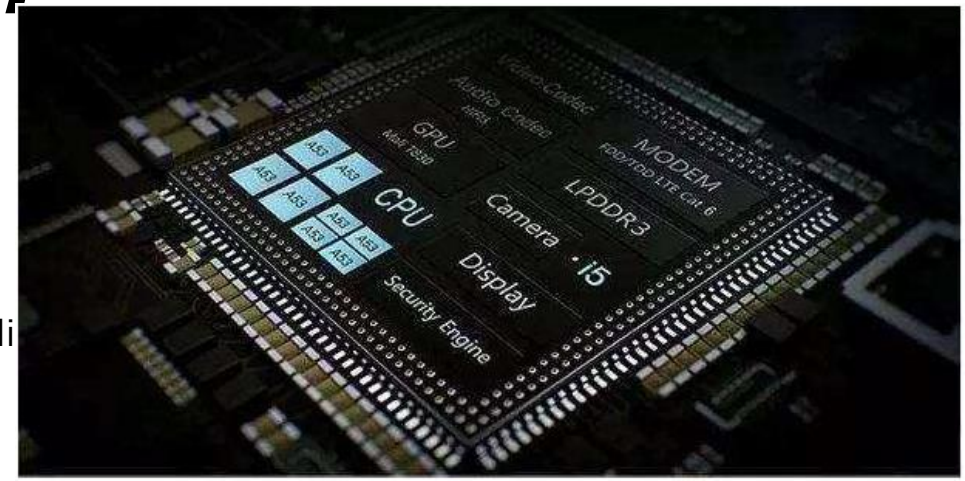
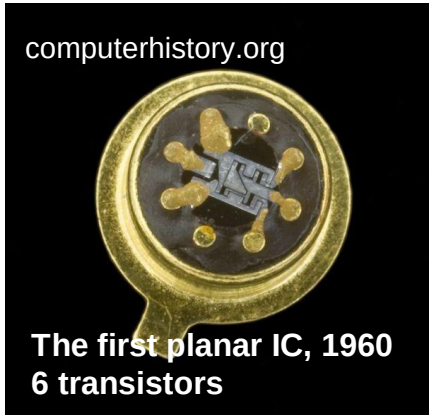
SoC technology, examples and business stakeholders

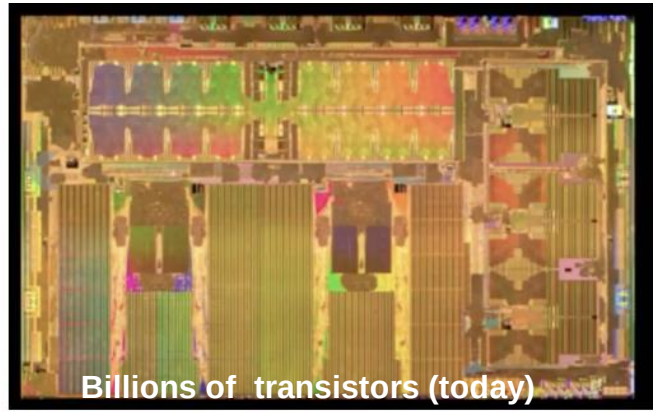
SoC: System on Chip



Components of the systems

- Functionality on silicon die
  - Digital logic to implement CPUs, Peripherals, communication protocols, interconnect, application specific accelerators
  - Internal memories
  - High speed analog circuits for clock generation, high speed interfaces, Radi circuits, etc.
  - Circuits to drive external pins of the IC
- Infrastructure on die
  - Routes on silicon to connect all above
  - Power grids
  - Structures for design for testing (DFT)
- Functionality stored and/or loaded to memories: Software
- Connections outside world
  - Package and bonding wires between die and pins
  - Dissipating the heat





IC technology:
The enabler for the increase on Integration during the time

- Increased amount of integration enabled by advancements in IC technology
- Integration of different types of designs and methodologies: Standard cell digital logic, memories, mixed signals, CPUs and SW.

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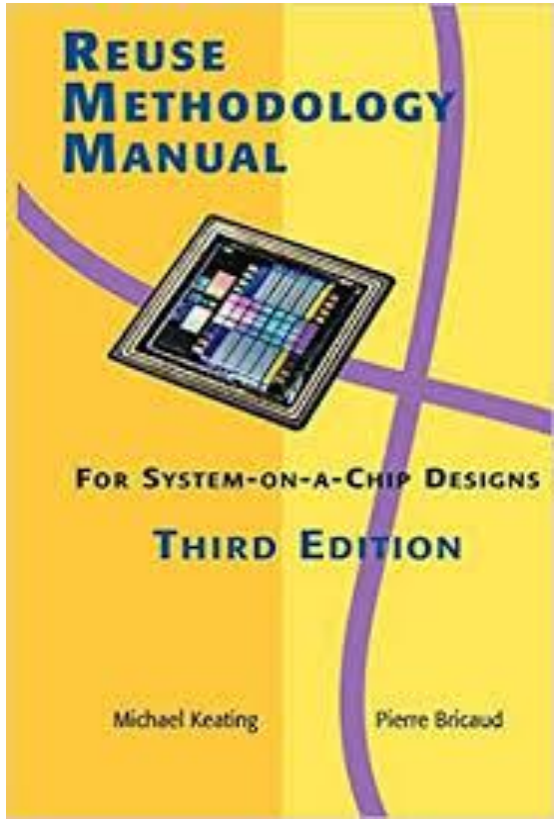
SoC: System on Chip

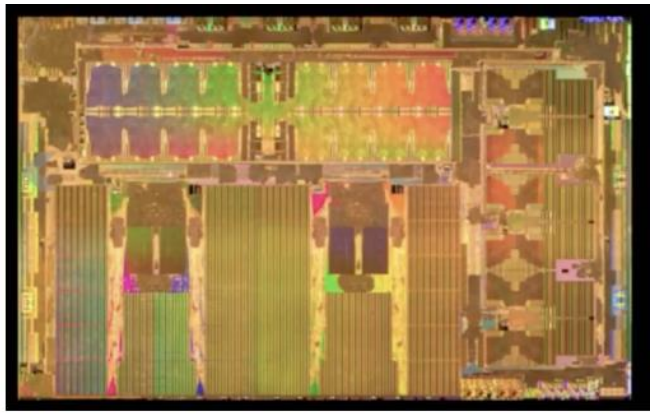
Methodology

- Reuse based design methodology
  - Standardization (attempts) for on-chip interfaces
  - Reuse inside companies
  - Reuse of commercial Intellectual Properties (IP is a model of the eventually physical sub-component inside chip)
    - Soft IP (Technology independent)
    - Hard IP (Technology dependent)
- Not a new thing. The dominating approach for past 20 years.



Benefits

- Reduction of the product costs with increased integration
- Added value through wider/better functionality
- Leading the innovations and markets through keeping technology and knowledge in-house
- Controlling bigger portion of the supply chain



Challenges

- Not a plug´n play
- Who has the system wide knowledge?
- Still Computing performance is typically memory bandwidth limited
- Multiple stakeholders involved in design
- Mixed signal designs and standard cell digital design not always feasible to utilize same technology

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Chip breakout examples

- Example A: Power consumption and cost optimization
- Example B:
  - Application specific HW accelerators
  - Application specific solutions creates need to deploy SoC technology on new areas
- Example C:
  - Not many can afford development and product cost
  - To increase the expected production volumes the solution is often more generic purpose platform
- Identifying application and target environment set's the base for technology selection and needed IPs
- Design and project complexity varies heavily per domain

Example domains / Attributes	A: IoT node	B: Domain specific AI SoC (e.g. machine vision)	C: Ultra High performance AI SoC
Computation performance	Low	Medium	High
Memory hierarchy, size and bandwidth	Minimized internal memory, low bw external memory, internal non-volatile memory	Application specific needs	Multi-level memory hierarchy, Maximized internal memory and high bw external memory connectivity
Hardware accelerators	Not used or minimal	Application specific designs	More generic AI computation clusters
Key targets	Low static power consumption, Minimized area (production costs)	Application and product specific PPA optimization	Performance
Interfaces	Low bandwidth, Minimizing amount of interfaces(cost optimization)	Application specific standard interfaces (camera, radar, radio, video)	Many high performance interfaces for different needs
Complexity (illustrative)	1x	50x	1000x

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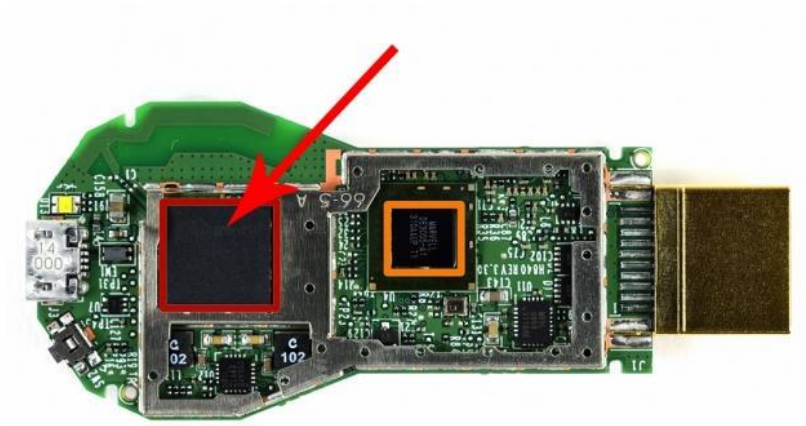
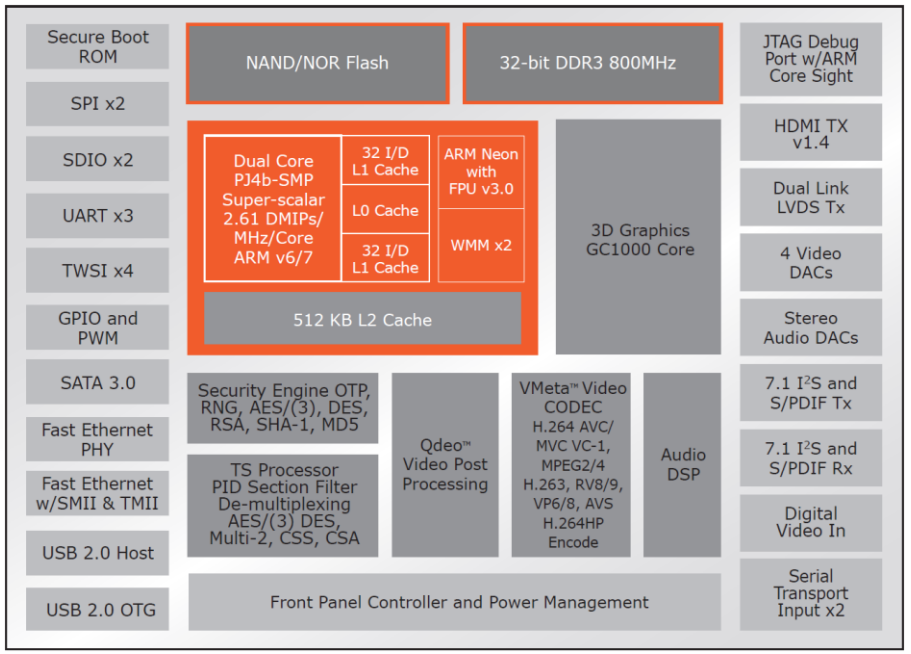
Consumer electronics product example





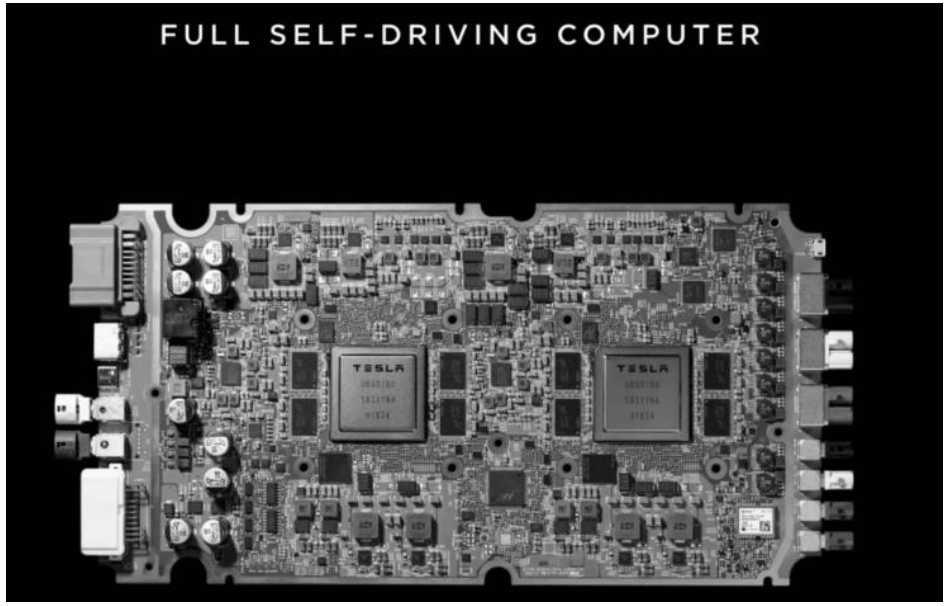
marvell armada 1500 mini plus for Google Cromecast (2013-present)

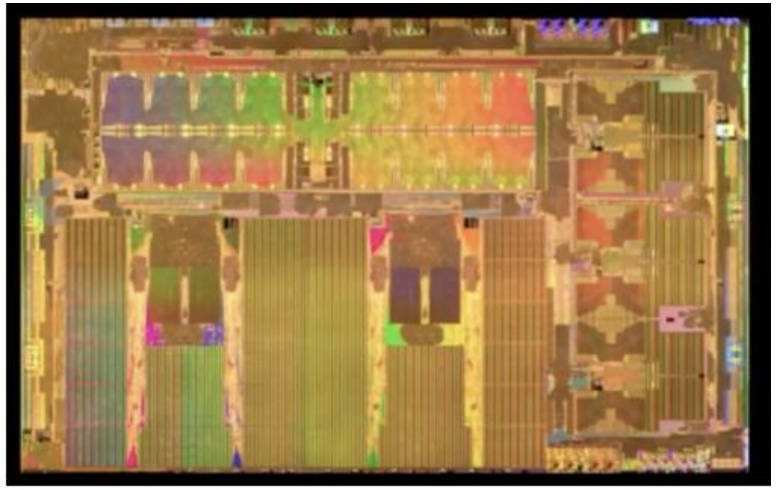
- Mass volume product
- Cheap product unit prize <50$
- Outsourced SoC design (Marvell)
- Moderate design costs: Standards and reuse
- Development costs are shared between multiple customers

Industry electronics product example

Tesla's First In-House Chip for Its Self-Driving Computer Is Built Using 14nm FinFET, With 250 Million Gates And Six Billion Transistors On A 260mm² Die

- Essential part of the product and not sold separately
- In house design and/or exclusive deal with sub-contractor
- Moderate volumes
- High unit price and price hided behind product costs
- Remarkably high development costs





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SoC development stakeholders

Business agreements and NDA agreements

IP providers companies

- Hard IPs
- Soft IPs

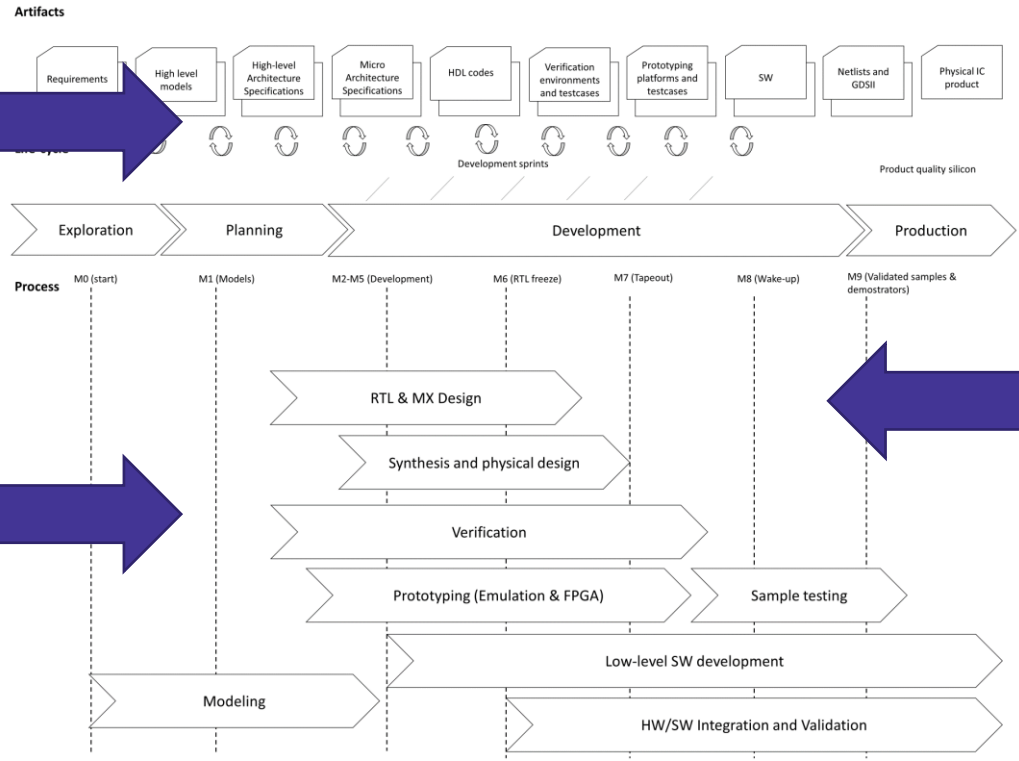
ASIC technology provider aka. vendor (TSMC, Global Foundries, Samsung etc)

- Technology models (libraries)
- Factories and manufacturing of dies

Outsourced assembly and testing (OSAT) companies

- Packaging
- testing

SoC development company



EDA companies

- Modeling tools
- ASIC implementation tools
- Simulators
- FPGAs and Emulators

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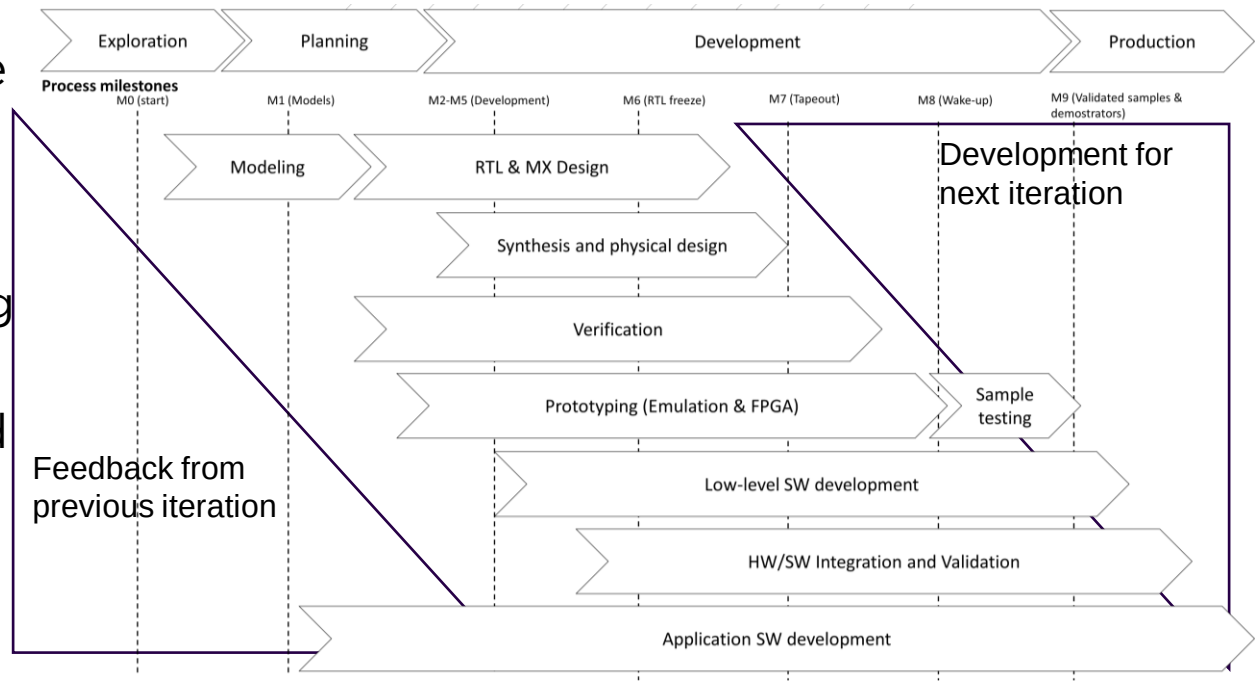
SoC Design flow

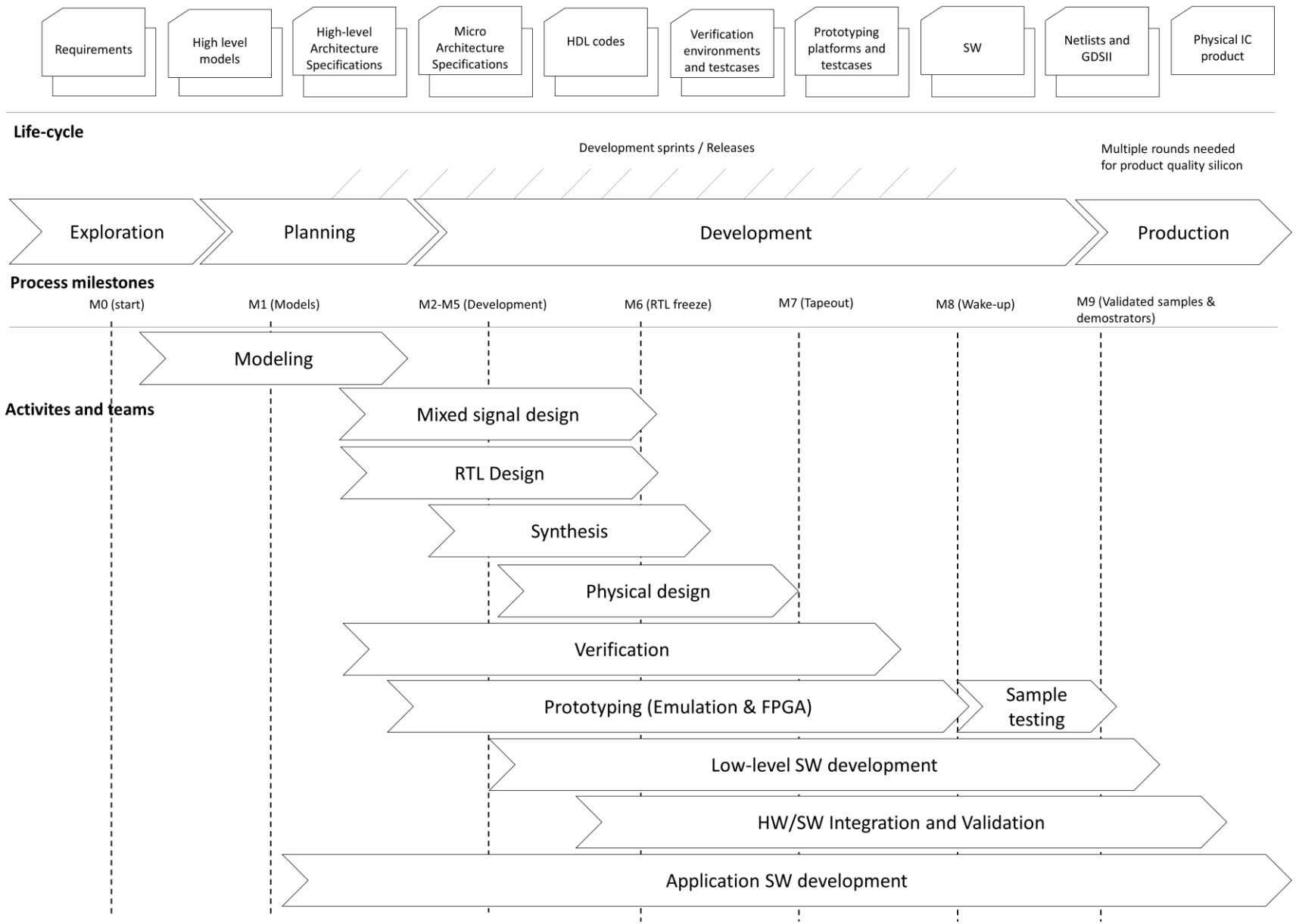
SoC design flow: Just before we start

- Flow and process descriptions are ***simplified models*** of more complex reality
- ***Flow description is not*** automaton or single tool which produces the chips. Actual work is done by humans with dedicated tools. Take good care of them!
- ***The purpose*** of the process descriptions are to set common understanding of the working environment and to help planning and managing of SoC projects
- ***Process is iterative*** although typically presented as single iteration
  - Iterations between multiple chip versions
  - Release/Sprint iterations during development
  - Continuous delivery to different teams



Well defined process doesn't guarantee success, but it near to impossible to succeed without.

SoC design flow: Overview



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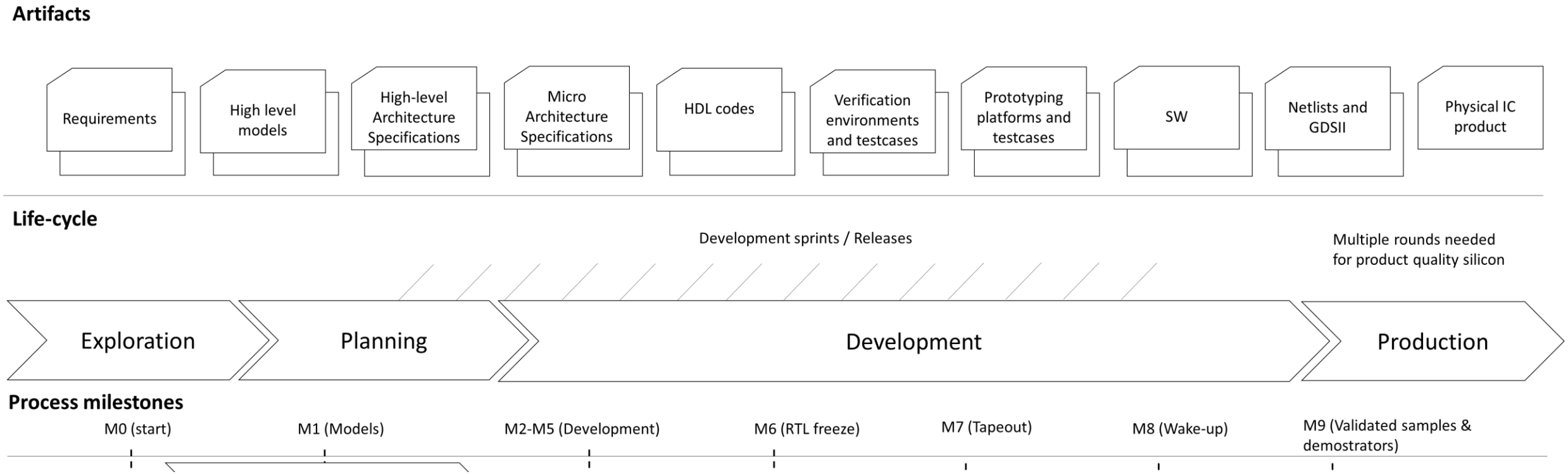
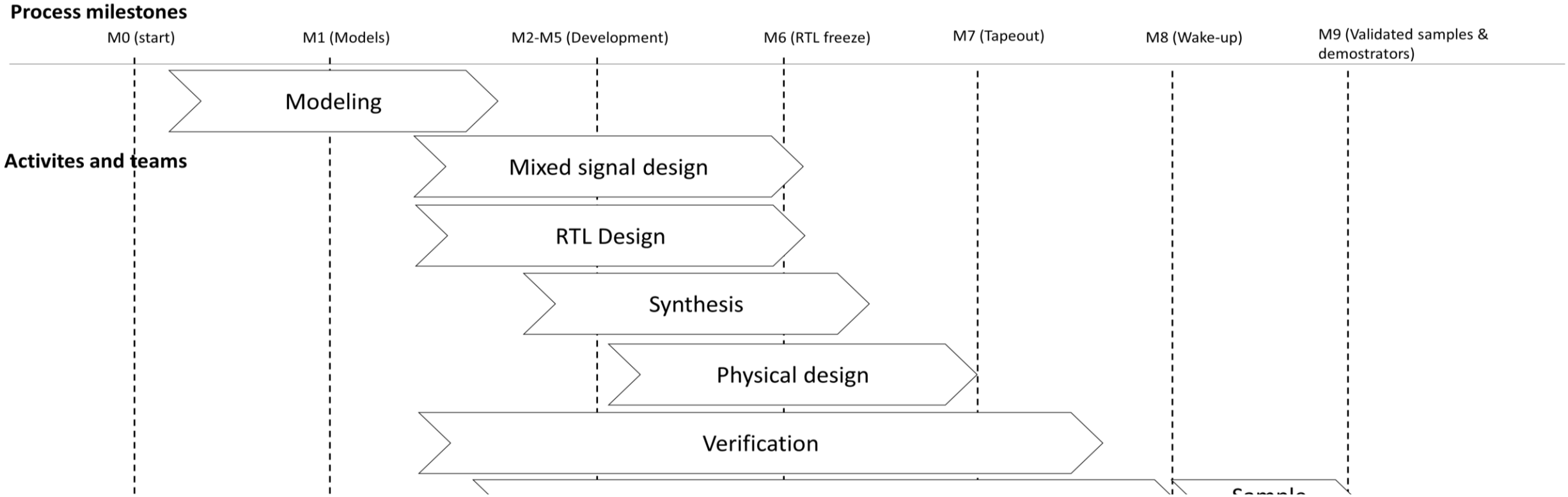


- ***Artifacts:*** Examples of typical deliverables produced in different phases of project
- ***Life-Cycles of the project :*** Exploration Planning, Development & production
- ***Process milestones:*** M0 – M9

SoC design flow: Overview



- ***Activities and Teams***
  - Each of the activity utilize different tools which constitutes specific tool flows: Mixed signal toolf low, RTL design tool flow …. Tens of different tools in total
  - Tool flows have many (5-10) main steps. Introduction to each tool flow would be workshop on their own and not covered today
  - Tool flows between different activities are coupled (I will return to this later)
  - Different tools and activities often utilize different programming languages
  - All domains have their domain specific key knowledge and expertise.
  - This all together means that SoC flow is multi- disciplined

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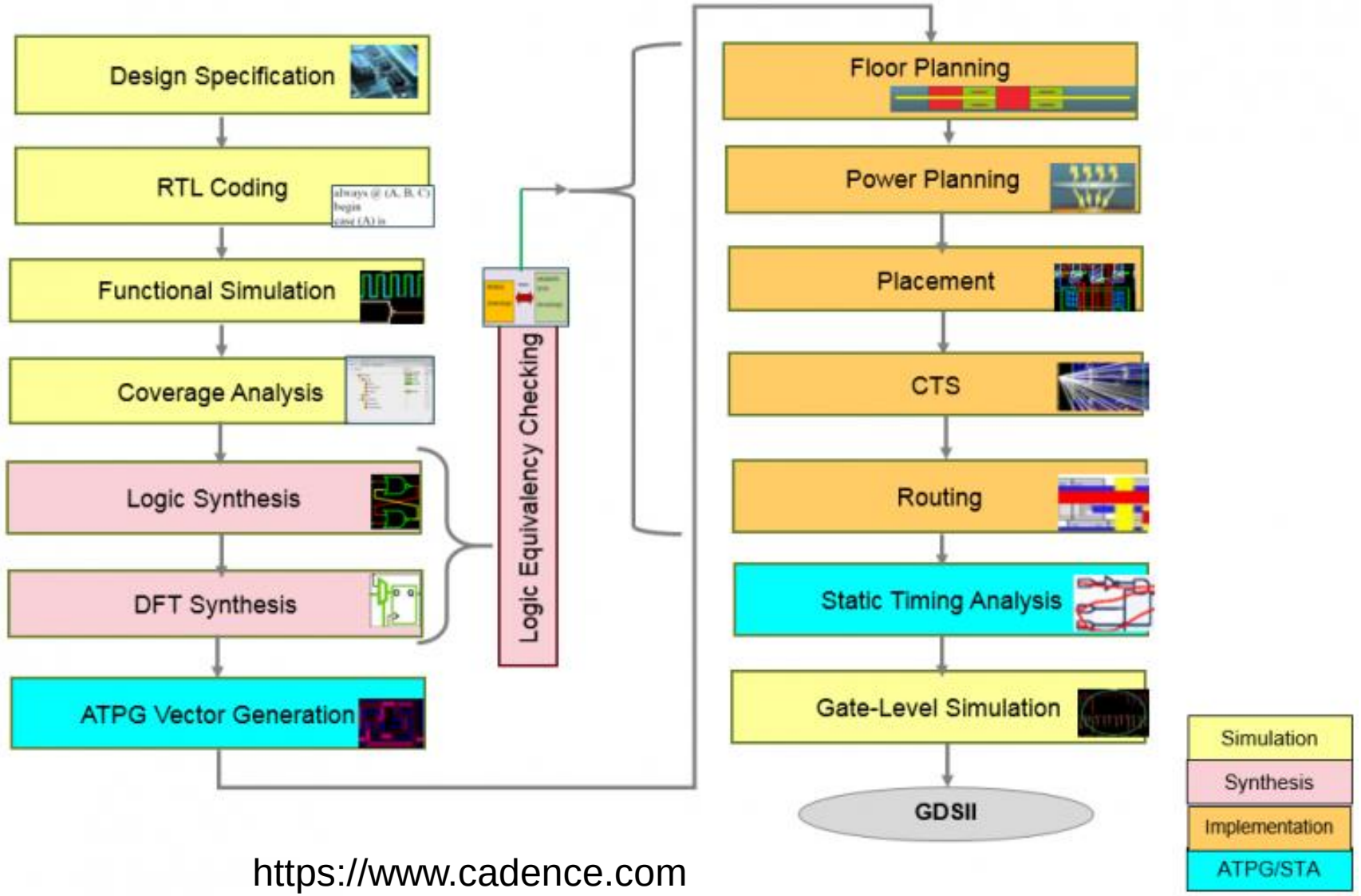
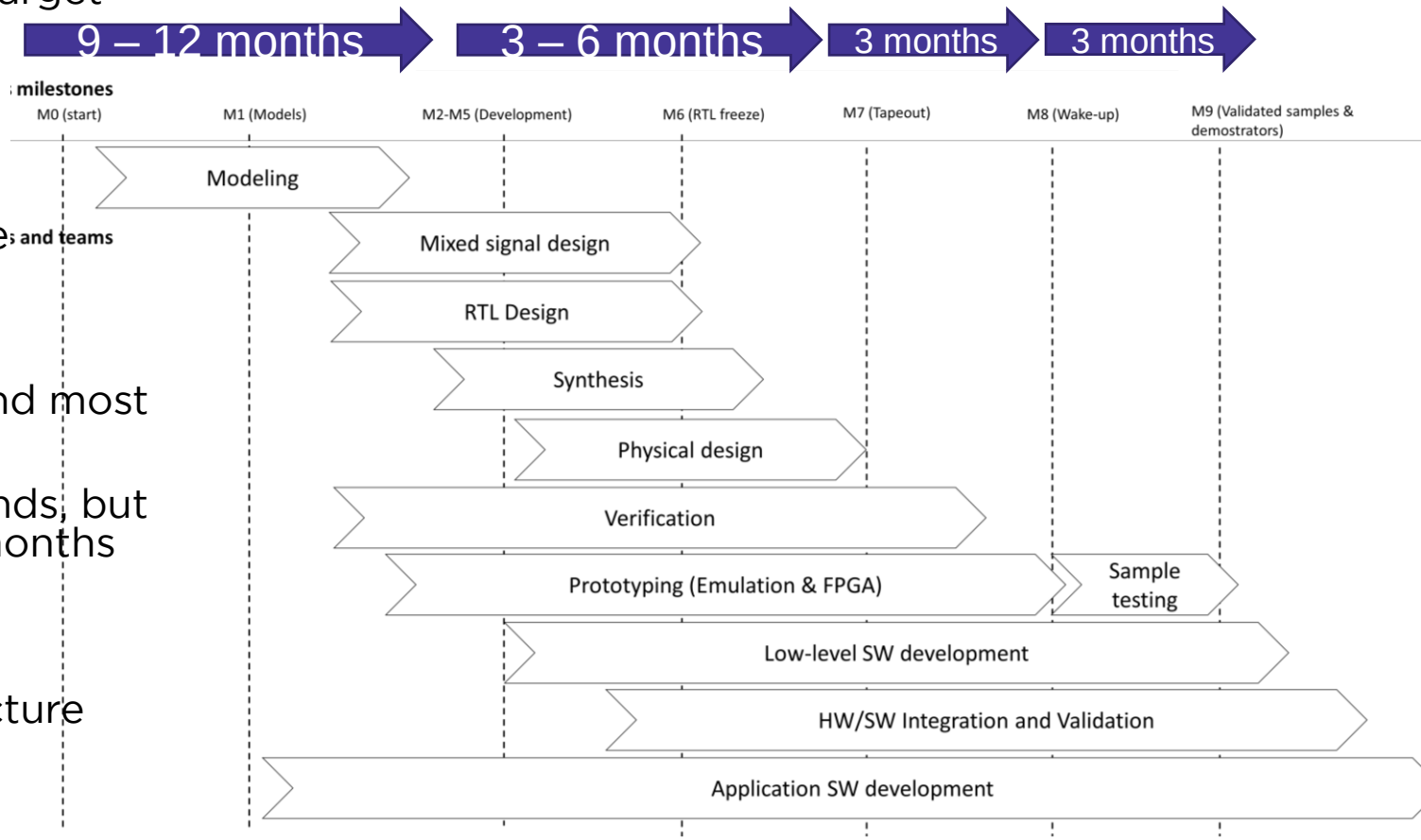
Overview of ASIC design tool flow



https://www.cadence.com

SoC design flow: Schedule

- Tapeout (M7): Handover of design database and decision to start the production is the key target and shapes process many ways:
  - You can't alter the design any more
  - Handover to external company
  - Big investment = big interest
  - It takes 3 months in average to prepare the fabrication



- Typical time from M0 to M8 is 1½-2 years and most of the project slip from planned schedule
- Product quality need typically multiple rounds, but additional rounds are much faster i.e. 4-9 months
- Being better on time requires that you
  - Decide technology provider early
  - Have needed tools and other infrastructure
  - Start of development with uncomplete models (agility)
  - Have needed knowledge and human resources

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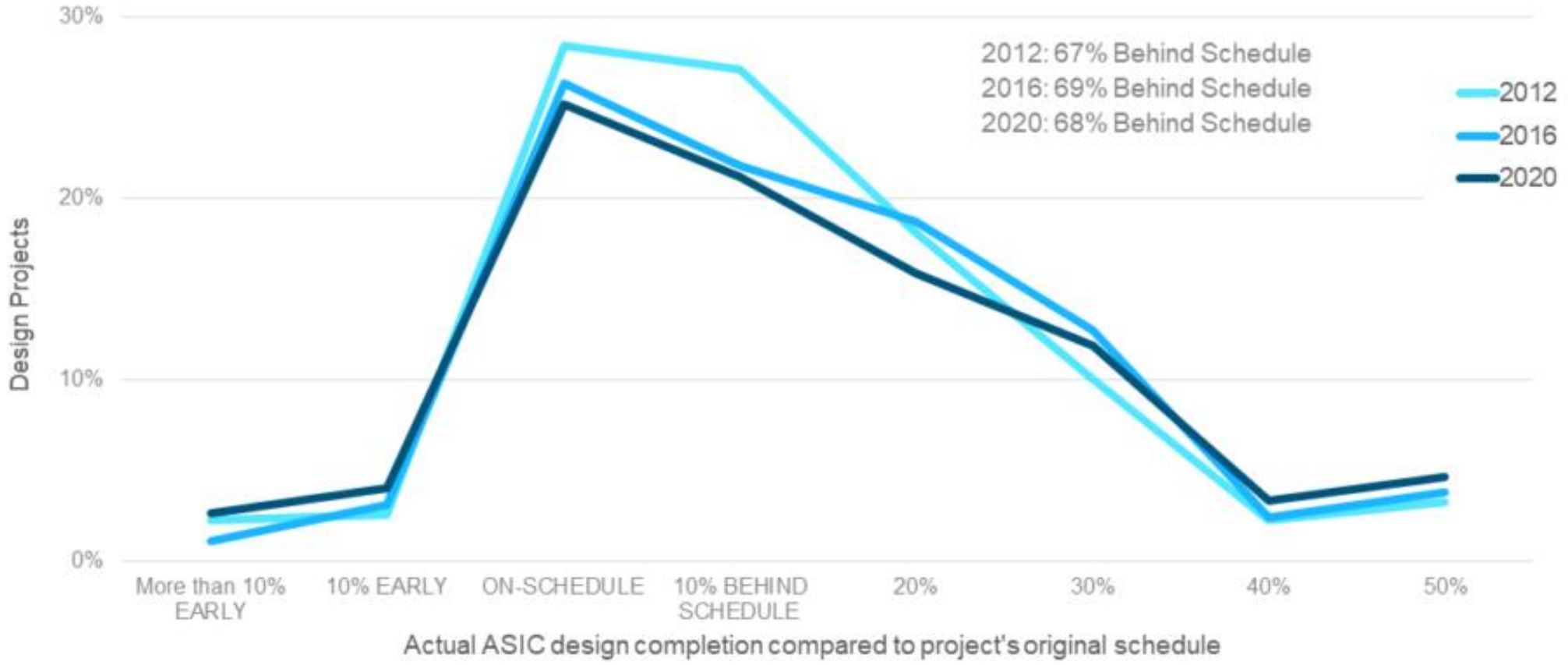
Wilson Research Group Functional Verification Study 2020

ASIC Completion to Project's Original Schedule



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

SIEMENS

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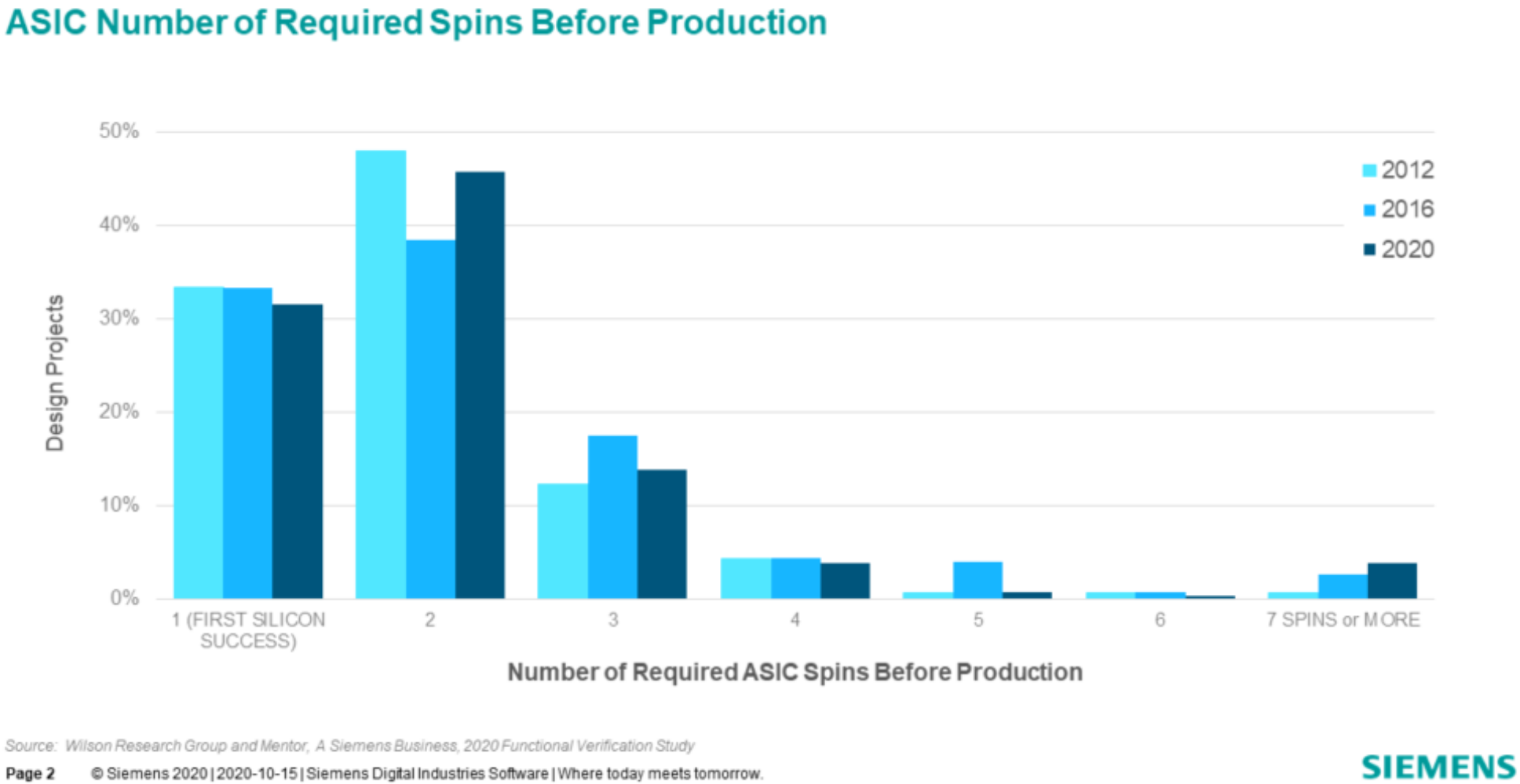
Wilson Research Group Functional Verification Study 2020



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

SIEMENS

The key question is that are spins planned
or surprises caused by quality flaws?

System Design: Exploration, planning, modeling

Exploration: Understanding the ***requirements*** and ***target ASIC technology early*** to gain understanding about the feasibility and limits of the system implementation

Modeling and models: Estimating the system power, performance and area (PPA)

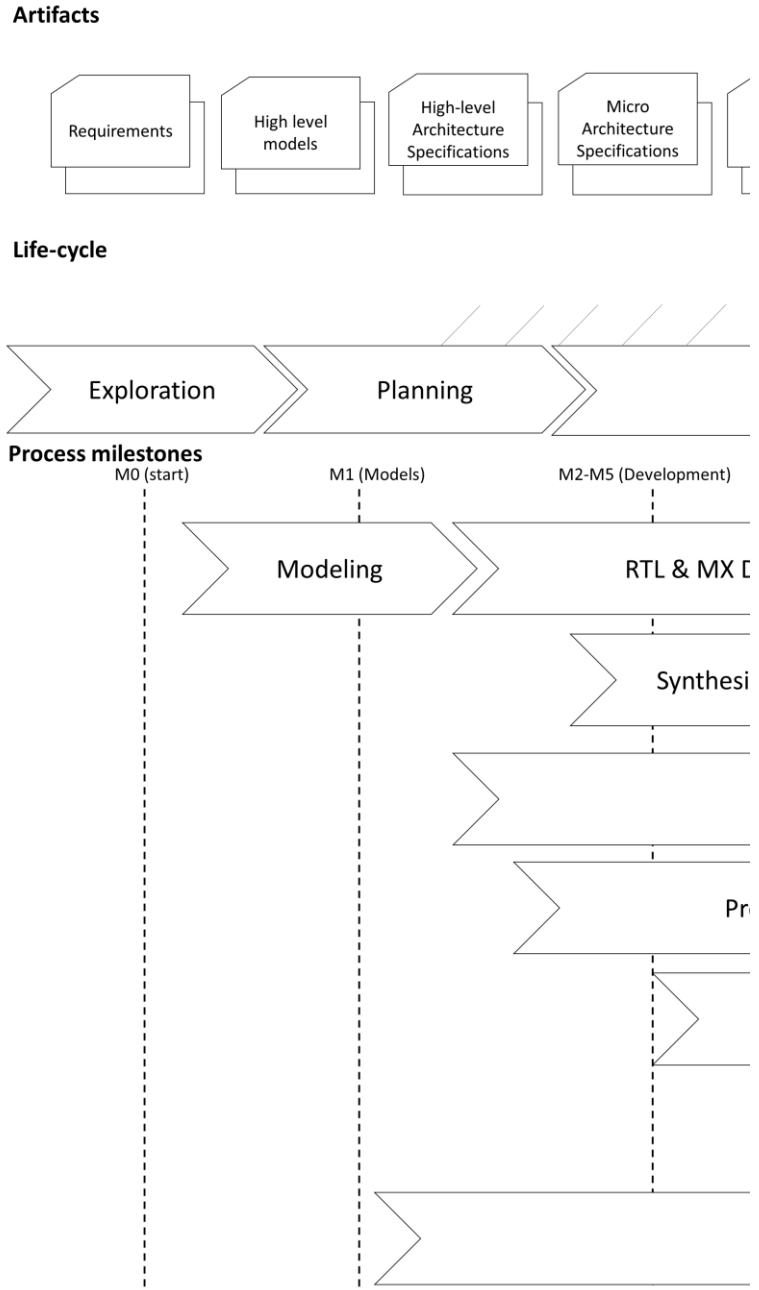
- Executable simulation models
- Non-executable models e.g. Excel calculations
- Knowledge of the organization

Planning: Decisions about system architecture based on models

- HW-SW partitioning, HW architecture
- Decisions on Accepted/Rejected requirements
- Decisions of in-house development vs. outsourcing

Challenges:

- Needs wide crosscut of different domain expertise
- Not a single entity. Models, measures and tools are sub-domain specific (Radio, AI, CPU, Interfaces)
- Even executable models gives typically limited visibility to PPA because models describe the functionality, but not how it's mapped to target technology
- Direct reuse between models and development is limited
- Not a common academic topic. Topics on sub-component level are measurable



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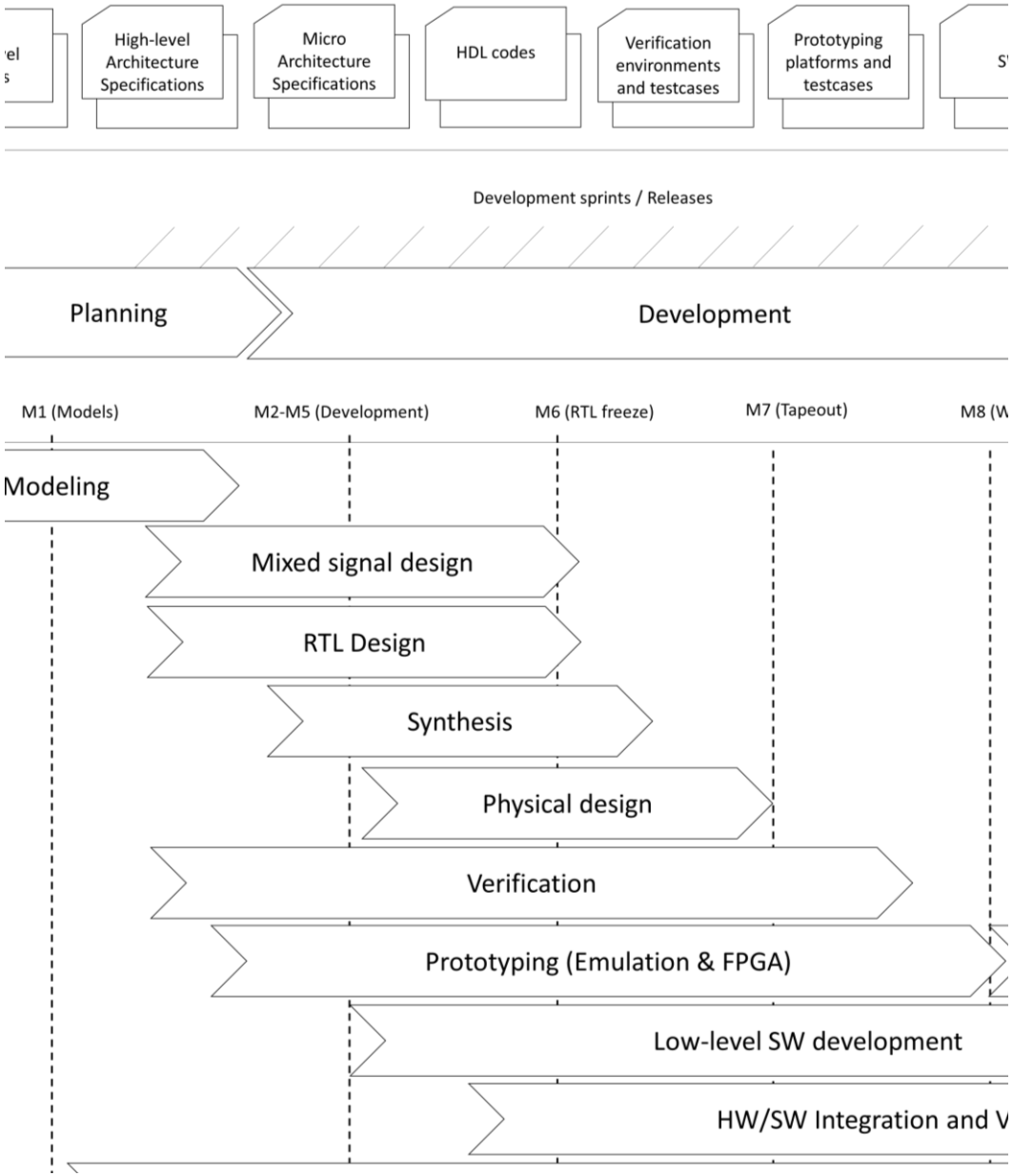
Digital design: RTL to GDSII & Verification

RTL to GDSII flow with standard cell libraries

- Register Transfer Level (RTL) ***Design***
  - ***technology independent*** structure and functionality defined with Hardware Description Languages (HDL)
- ***Synthesis*** from HDL to more detailed gate level representations to get feedback on timing, area and power
- ***Physical design***: Layout and internal routing of the chip. More detailed technology mapping
- ***Automation*** in synthesis and physical design means that tools find suitable solution automatically to meet set constraints such as timing.
- ***Verification:*** To guarantee correct functionality of models on different accuracies
  - RTL simulation
  - Gate level simulation
  - Formal equivalence checking
  - Formal model checking
- ***Prototyping:*** To provide faster platform for simulation and to test in real environments



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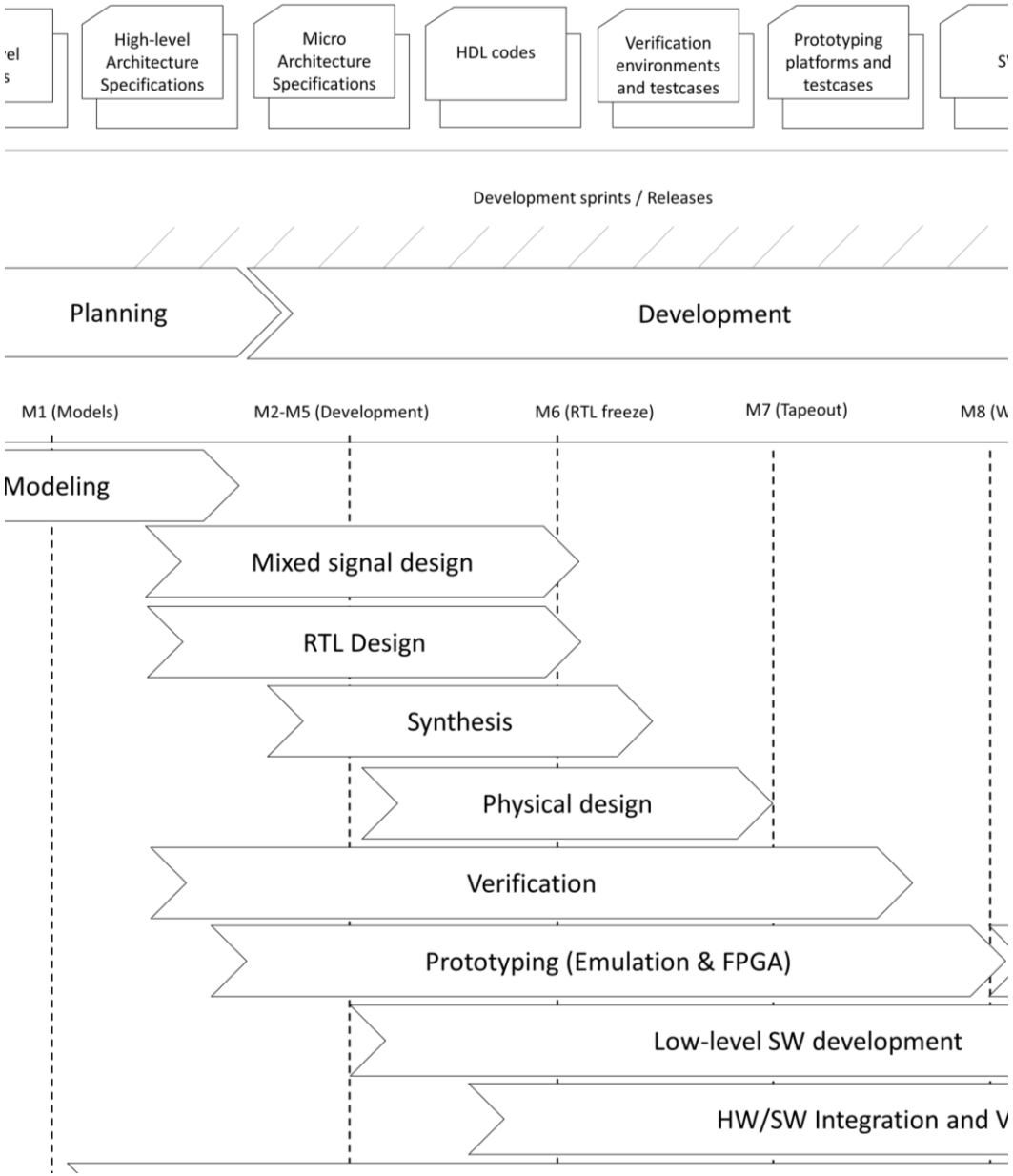
Analog and mixed signal design

Analog and mixed signal design with technology library components and custom cells

- Needed in fast circuits such as clock generation, memory interfaces, communication interfaces, radios etc.
- Different components can be partly generated, but quality of the results needs to be validated separately. Manual iterative process to meet result targets.
- Digital design and analog design block are integrated together in physical design tool flows
- Circuit simulations to verify functionality and quality of the results
- Simulating analog and digital design together is possible, but slow. Typically, abstracted models of analog components are used when simulating the chip
- ***Technology dependent implementation***
- Because many SoC interfaces are standard specific companies are providing often these designs



SoC design flow: Development, Software

SoC software: Low-level ***hardware specific software*** development

- Programming of bare-metal applications (no OS), HW APIs, OS Device drivers, OS adaptation layers to hide details of the HW.

Application software development HW/SW integration and validation

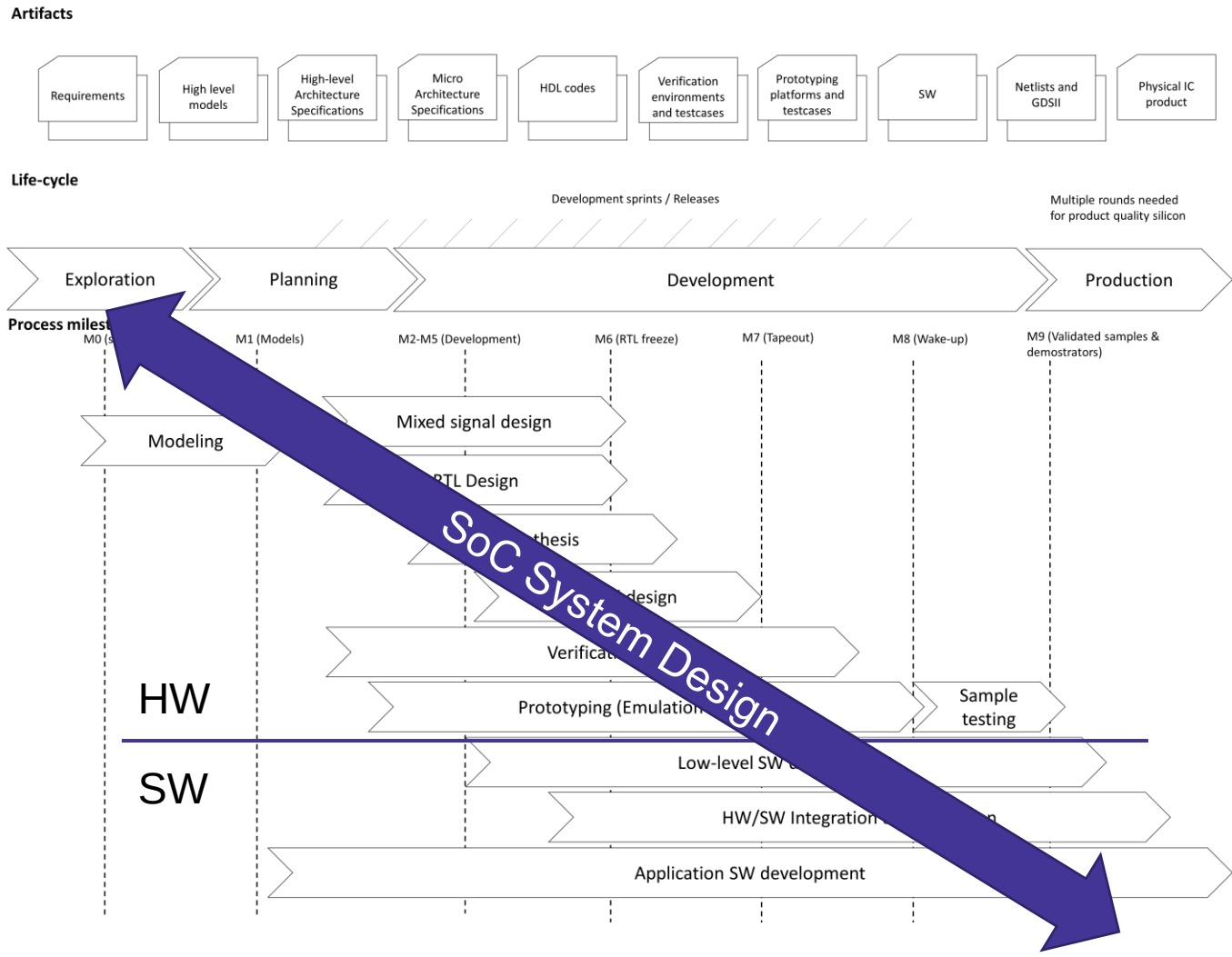
- Less HW dependent SW
- Validation of assumptions made already in modeling phase and can't be done without HW.

Challenges:

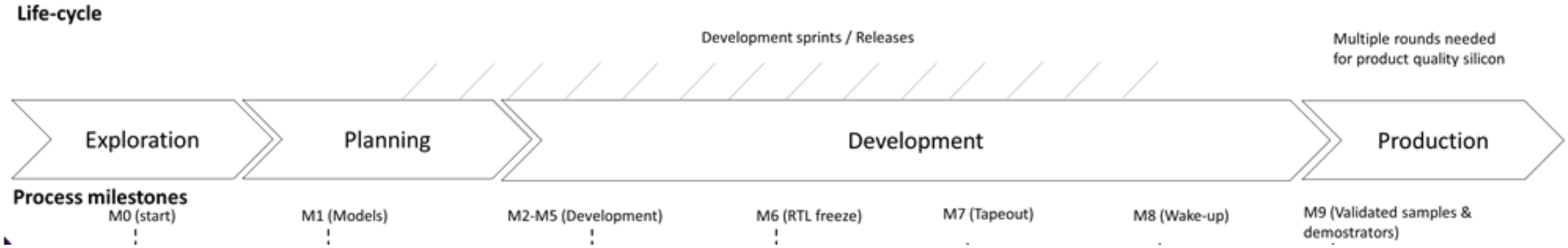
- You still do not final chip in hands
- Selecting suitable platform for HW and SW co-simulation?
  - RTL simulator is accurate but is too slow and has unnecessary complexity for SW development
  - Additional models such as prototyping and emulation increases the maintenance and complicated synchronization of work
- Synchronization challenge: HW development on-going on same time

Sample testing: Validation of real chips with SW

- Fast real time operation, but very limited visibility to debug hardware



SoC design flow: Summary



Inaccurate models – more accurate models – real device

HW Changes possible – HW changes hard – HW changes very limited – HW changes impossible

Fast inaccurate simulation – Slow accurate simulation – Faster simulation in complex platforms - Real time execution with limited visibility

Combining head and tail – All activities on-going parallel - Combining tail and head

Secured funding - Good plans – Great development team – Happy customer ☺

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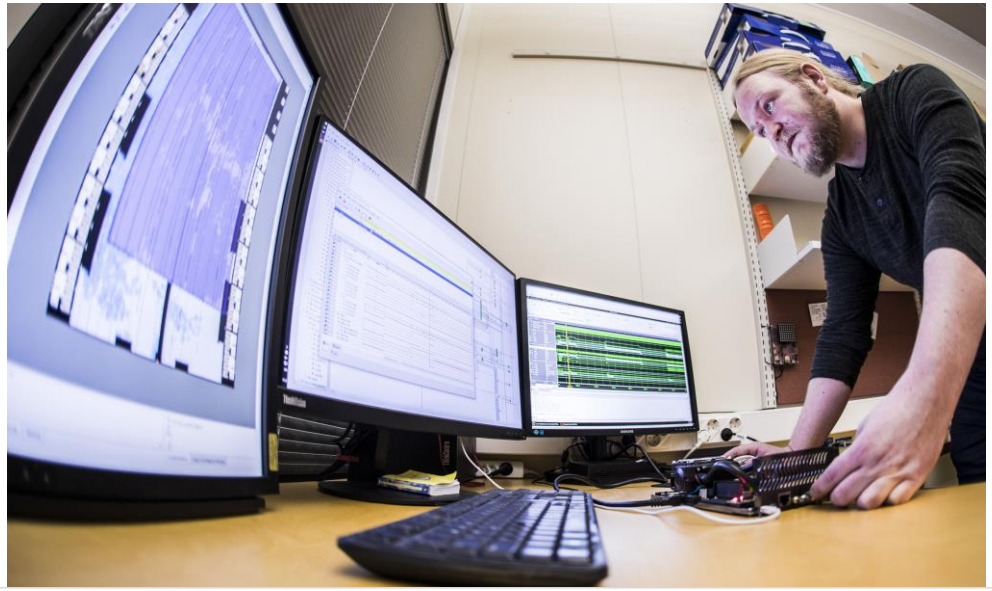
SoC Hub Update

Timo Hämäläinen

SoC HUB

SoC Hub update

- Current news on SoC Hub progress
- Contributors
- SoC Hub as a project
- Schedule
- Infrastructure
- Team



SoC Hub chip 2021 subsystems

Top architecture	Medium performance CPU	DSP co-processor	Top level peripherals	Clock generator	Ethernet v1
System control CPU	High performance computing multicore	On-chip interconnect	Chip to chip	AI accelerator v1	

SoC HUB Founding partners

Applications and business development partners	IP blocks and subsystem contributors	System integration and methodology partners

BUSINESS TAMPERE

CARGOTEC

procemex

Wapice

CoreHW

FLEXIBILIS

VLSI SOLUTION

NOKIA

SIRU INNOVATIONS

Tampereen yliopisto Tampere University

SoC Hub schedule

	2020 1	2020 2	2020 3	2020 4	2020 5	2020 6	2020 8	2020 9	2020 10	2020 11	2020 12	2021 1	2021 2	2021 3	2021 4	2021 5	2021
Funding, project, dissemination	Vision setup; partner search started	Project proposal kick-off	EAKR application submitted	BF project plan started	BF application submitted		EAKR project accepted	EAKR project started	BF application revised	BF project accepted and started		SoC Hub launch		SoC Hub webinar #1	S4E collaboration starts		SIG created
Agreements														EDA tool agreements	IC Tech agreements	IPR agreements	
Infrastructure	TAU EDA tools ready	Sharepoint, Teams setup	Gitlab, Redmine setup	EDA tools selection	Standalone FPGAs setup	CI pipeline setup started	IT architecture plan				Servers ordered		Collaboration EDA architecture	Server installs	IC Tech libraries	FPGA emulation boards	Sample testing PCB
Chip #1			RISC-V selection	Archi-tecture plan	Sub-system FPGA prototyping started				Sub-systems freeze		RTL freeze		App plan	SW archi-tecture	Emulation starts	Backend starts	Chip #1 tapeout; BSP, SDK ready

9 and 11 months from vision to funding decisions

23 business entity agreements signed + personal NDAs

12 months from 1st SoC draft from scratch to starting backend (11 subsys)

SoC HUB Infrastructure – status 3/2021

- Simulation capacity
  - Front + backend servers XEON Gold, virtualized 4x[24CPU, 32GB RAM], shared 15TB SSD
  - Desktop PCs x64: 40x[8CPU, 32GB]
- Emulation capacity
  - Xilinx UltraScale VCU118
  - Zynq UltraScale+ MPSoC ZCU104 (sample testing PCB companion)
  - Xilinx Pynq (smaller digital IP functional prototyping)
  - Remote accessible
- 22nm ULL IC technology from TSMC/IMEC
- Test lab for high-speed electronics and communications
- Tooling from leading EDA vendors Cadence, Siemens/Mentor, Synopsys and others
- Commercial IPs from partners, open-source IPs and tools
- Collaboration tools (repositories, issue system)

Per subsystem run / phy design)

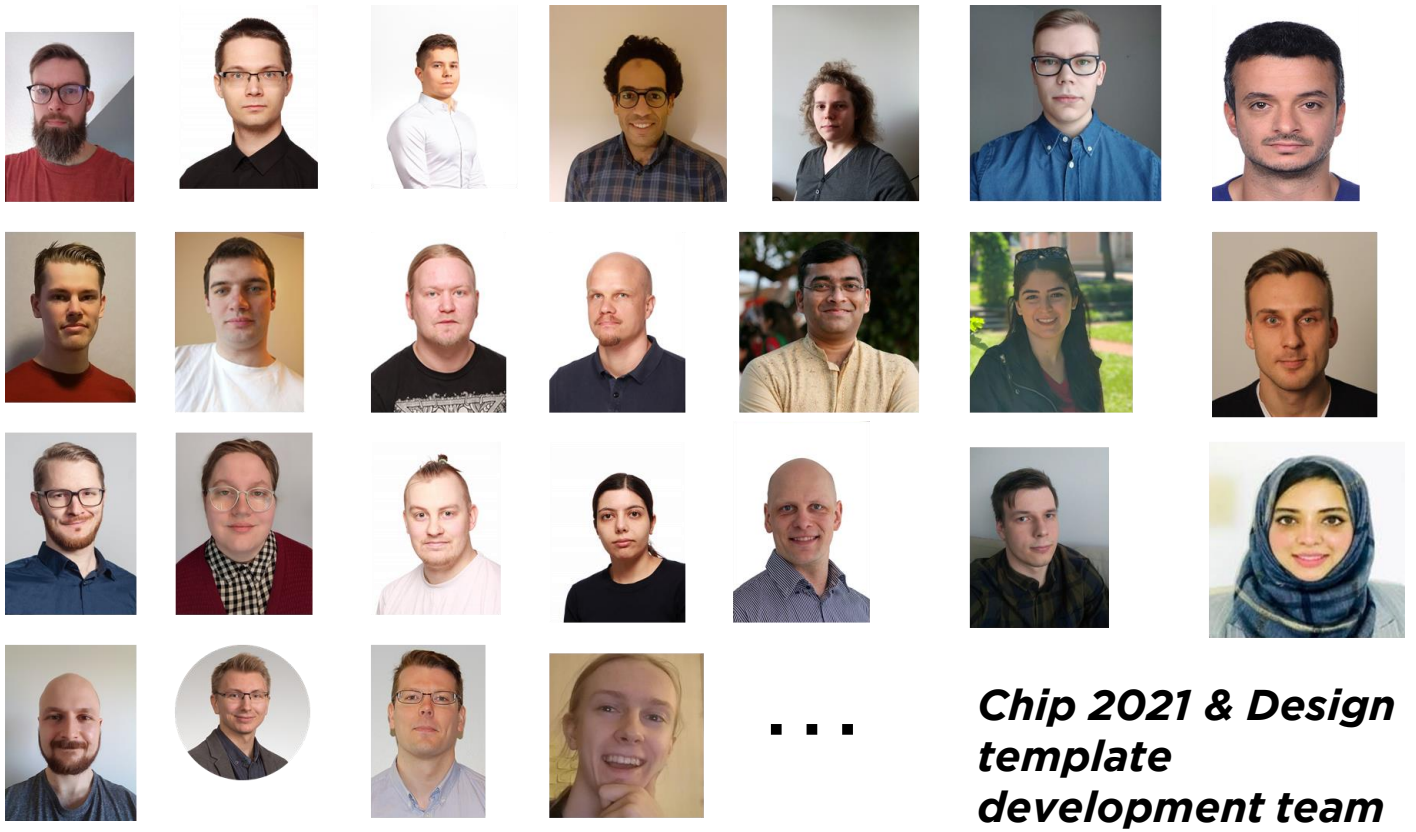
- 8-16 CPU cores
- 32GB RAM
- For top: 256-512GB RAM

TAU's open source tools:

- Kactus2: register map; IP packing and integration;
- TCE: ASIP generator

The team – status 3/2021

6x founding professors representing computer engineering, wireless communication, embedded systems and SW, electronics, IC design



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Chip 2021 & Design template development team

Founding professors + 23 researchers at TAU 3/2021 + staff members at companies = ~50 persons in seamless development team

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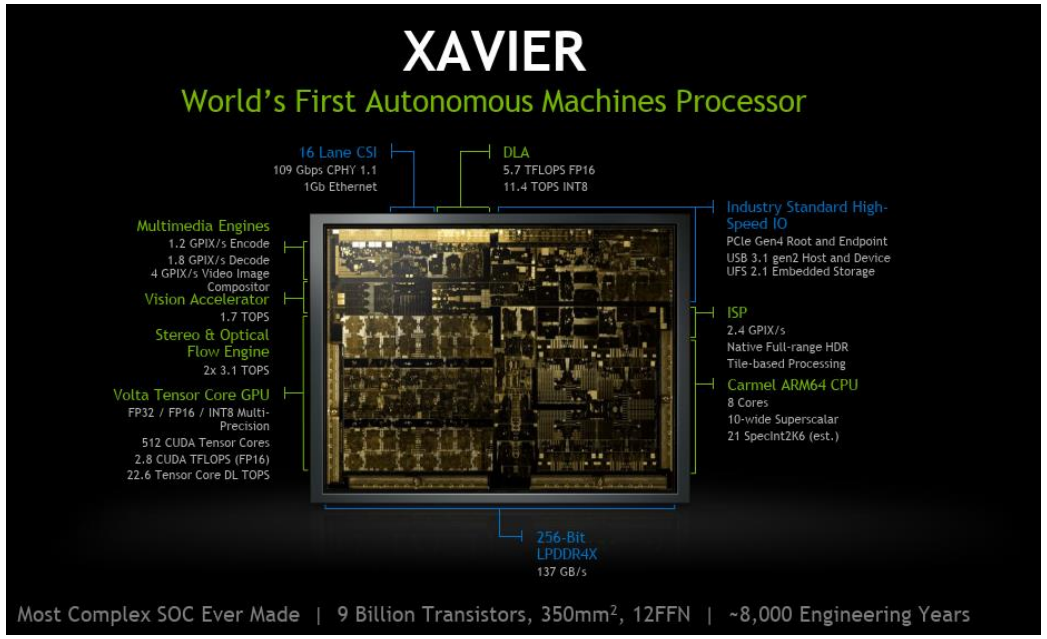
Part II: SoC Project Management

Design, infrastructure, resources, schedule and costs

Antti Rautakoura

Scale of the complexity and costs



https://old.hotchips.org/hc30/1conf/1.12_Nvidia_XavierHotchips2018Final_814.pdf

SMIV: motivation and chip overview

SoC platform for architecture and systems research

Test chip details

- 25mm² die area (5mm x 5mm), TSMC 16nm FFC
- Half a billion transistors, 72.2 Mbit of SRAM, 7 clocks, 5 power domains
- First academic chip to feature Arm Cortex-A class CPUs
- All-digital GHz+ on-chip clock generation and chip-chip link
- Custom 672-pin flip-chip BGA package

Very short design, validation and implementation cycle

- 7 people (4 PhDs and 3 post-docs) in about 9 months (final IP came in 6 weeks before tape out)

https://old.hotchips.org/hc30/1conf/1.10_Harvard_Whatmough_Hotchips_2018_0.7.pdf

	Xavier	SMIV
Transistors	9 Billion	0.5 Billion
Technology	12 TSMC FFN = FinFET NVIDIA	TSMC 16nm FinFET Compact
Purpose	Multi purpose high performance AI platform	Academic demonstrator of modern ARM cpu + custom AI accelerator
Interfaces	109G CPHY, 1G Eth mPCIe gen 4, USB 3.1, 256bit LPDDR4	GPIO based chip-to-chip
Engineering years	8000	7x9/12 = 5,25
Transistors/engineer year	1,125M	95M

- Be careful with you wishes and promises!
- Typically, biggest and boldest gets more attention

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Understanding the challenges

RTL to GDSII flow challenges on project level

- Dependencies to external providers
- Dependencies of the tool flows: All of them are dependent on RTL design
- Complexity of the design: 50 sub-blocks -> 50 sub activities inside RTL design -> 50 verification activities
- Non elasticity of the RTL model compared to SW.
- Long run times of the tool flows. From multiple days to multiple weeks with server class expensive x86 machines
- Dedicated tools and expertise per area

Symptoms

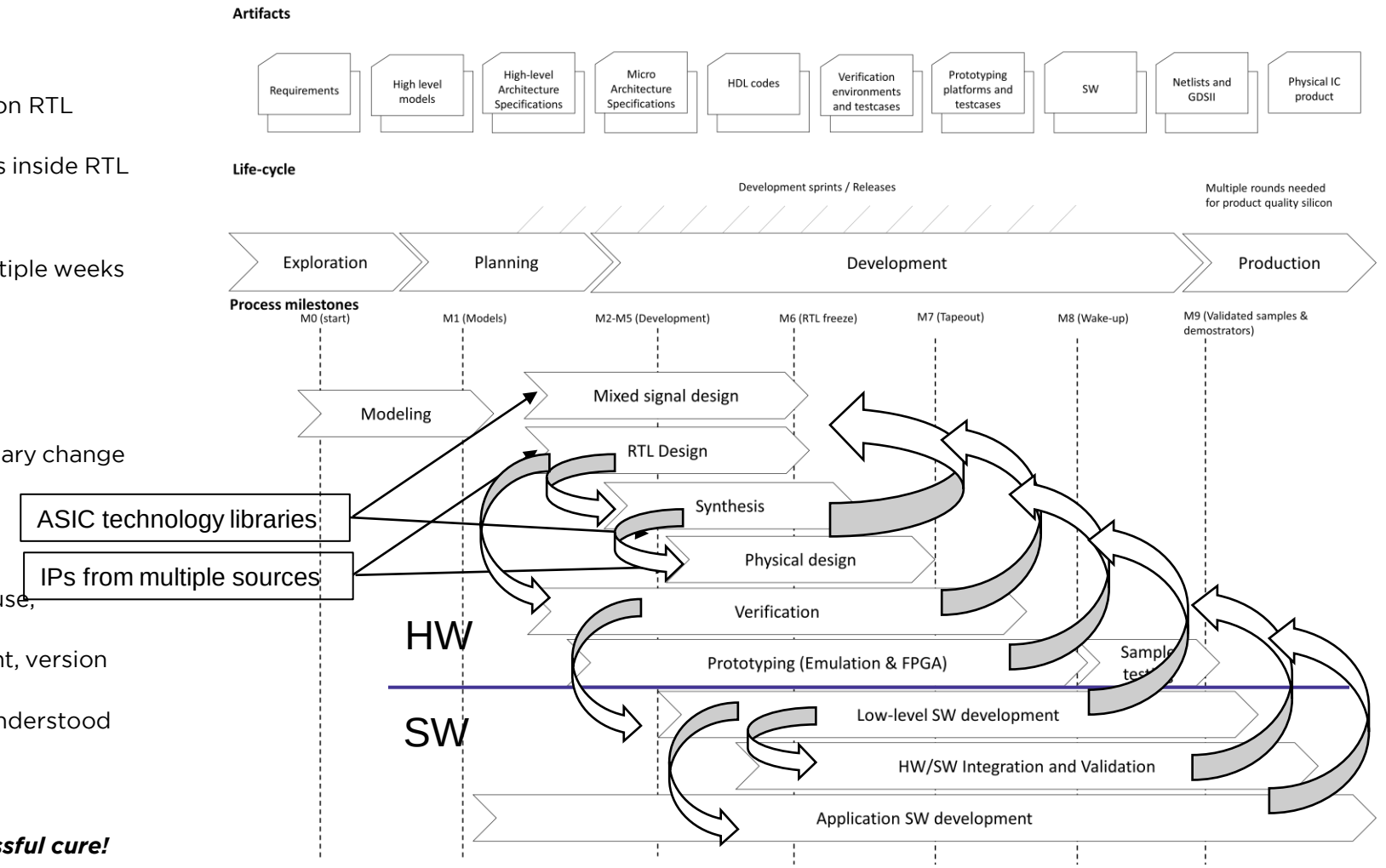
- Limited number of major iterations possible
- Cost of bugs realize already inside development. Unnecessary change can lead to wasted iteration
- Lot of communication is needed between activities

Potential cures

- Long life-cycle platform architecture to enable efficient reuse, knowledge sharing and correct by construct practices
- Disciplined work: Up to date information, data management, version control, milestones as quality control to avoid surprises
- Well understood process so that causes of shortcuts are understood
- Shortest distance to verification
- Automation to avoid extra communication

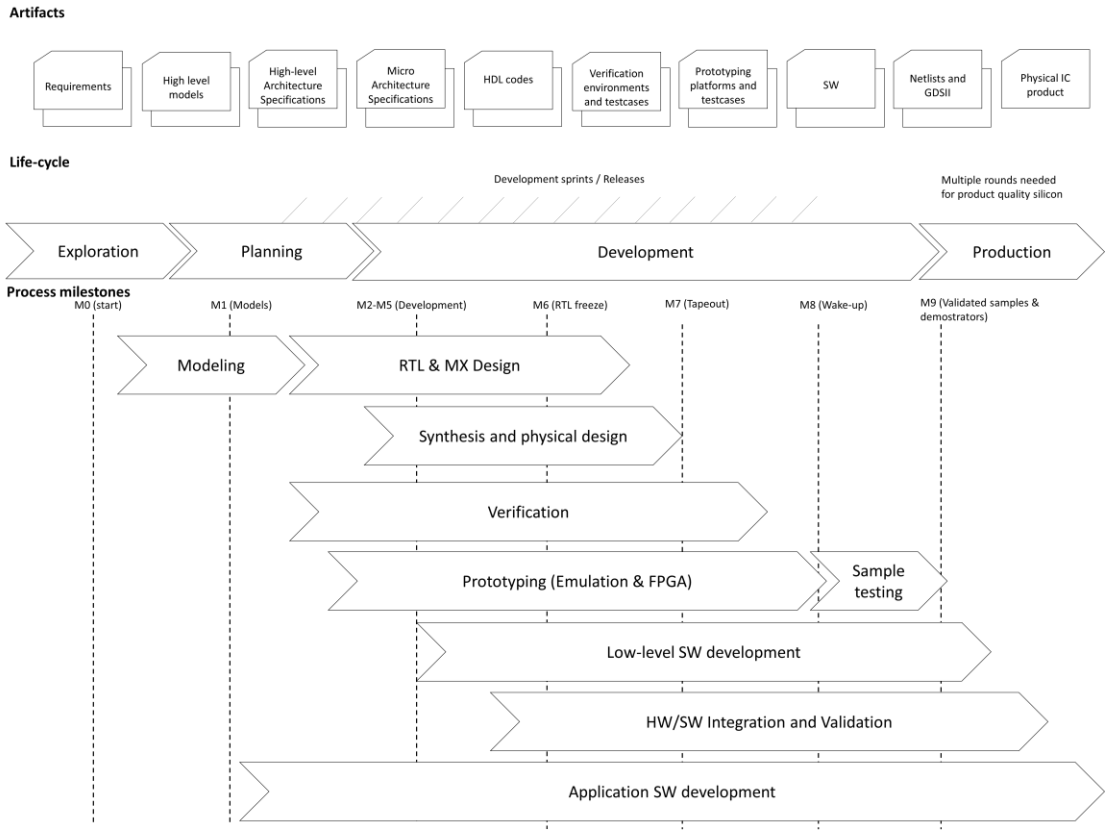
Recognizing and admitting the challenges is the key for successful cure!

When you have competence teams and high built-in quality, magically complex projects becomes possible



SoC design flow: Investments

- Major non-recurring (NRE) investment decisions are at:
  - Early investments (M0-M1): Setting your business environment
    - Agreements about potential outsourcing (design services)
    - Frame agreements with ASIC vendor (technology selection)
    - IPs, especially hard Ips
    - Prototyping devices
  - M7: Start of ASIC production.
- Recurring investments
  - Salaries for 5 - x00 professionals
    - SoC-hub invest on design template which targets to decrease work needed on longer run
  - EDA tool licenses
  - IT infrastructure to run the tools
- Managing mass production:
  - Balancing with demand – supply & production cost optimizations
  - Manufacturing needs to be ordered well in advance.
  - Predicting markets and preparing for unpredictable events such as environment catastrophes, trade wars etc.



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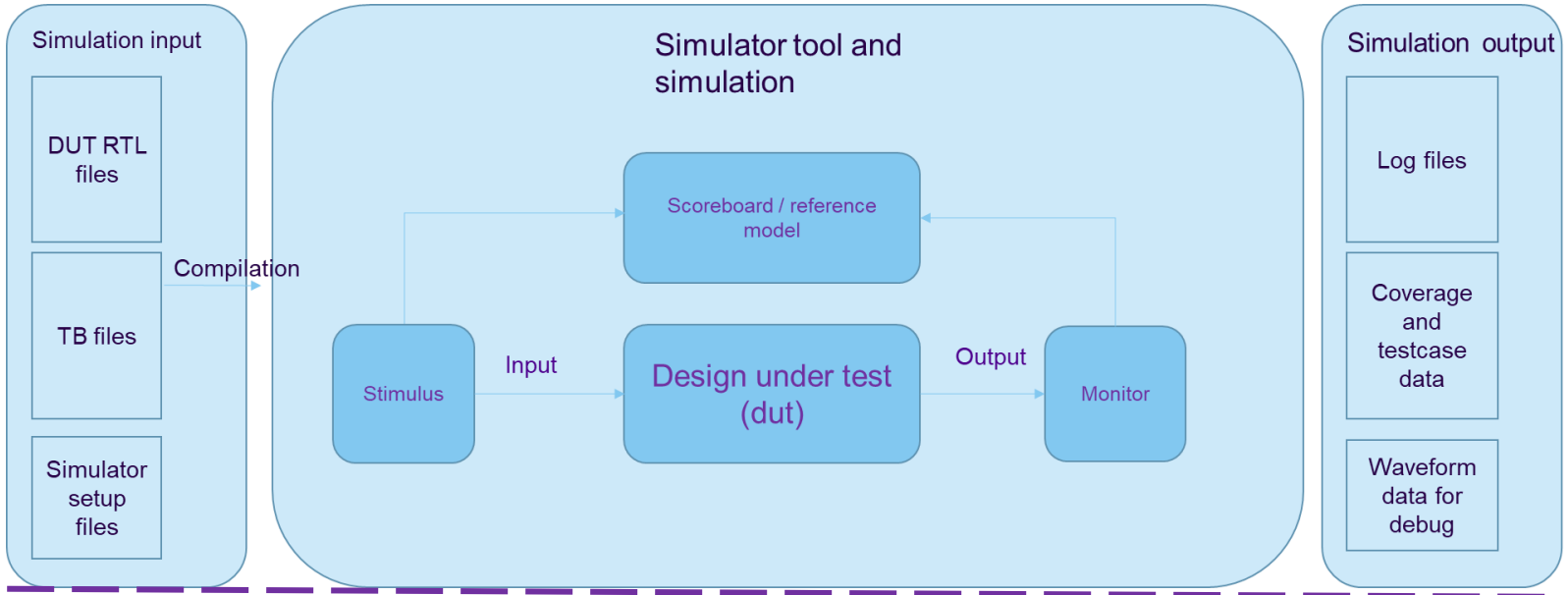
Design environment and skills needed

Artifacts and activities



Tools and infrastructure

Version control

Editors and IDEs

Compilation framework (e.g. Makefile)

Verification tools
Simulation tool: Modelsim/Questa, VCS, Incisive
Formal tools
Debug tools

Data management

Issue management

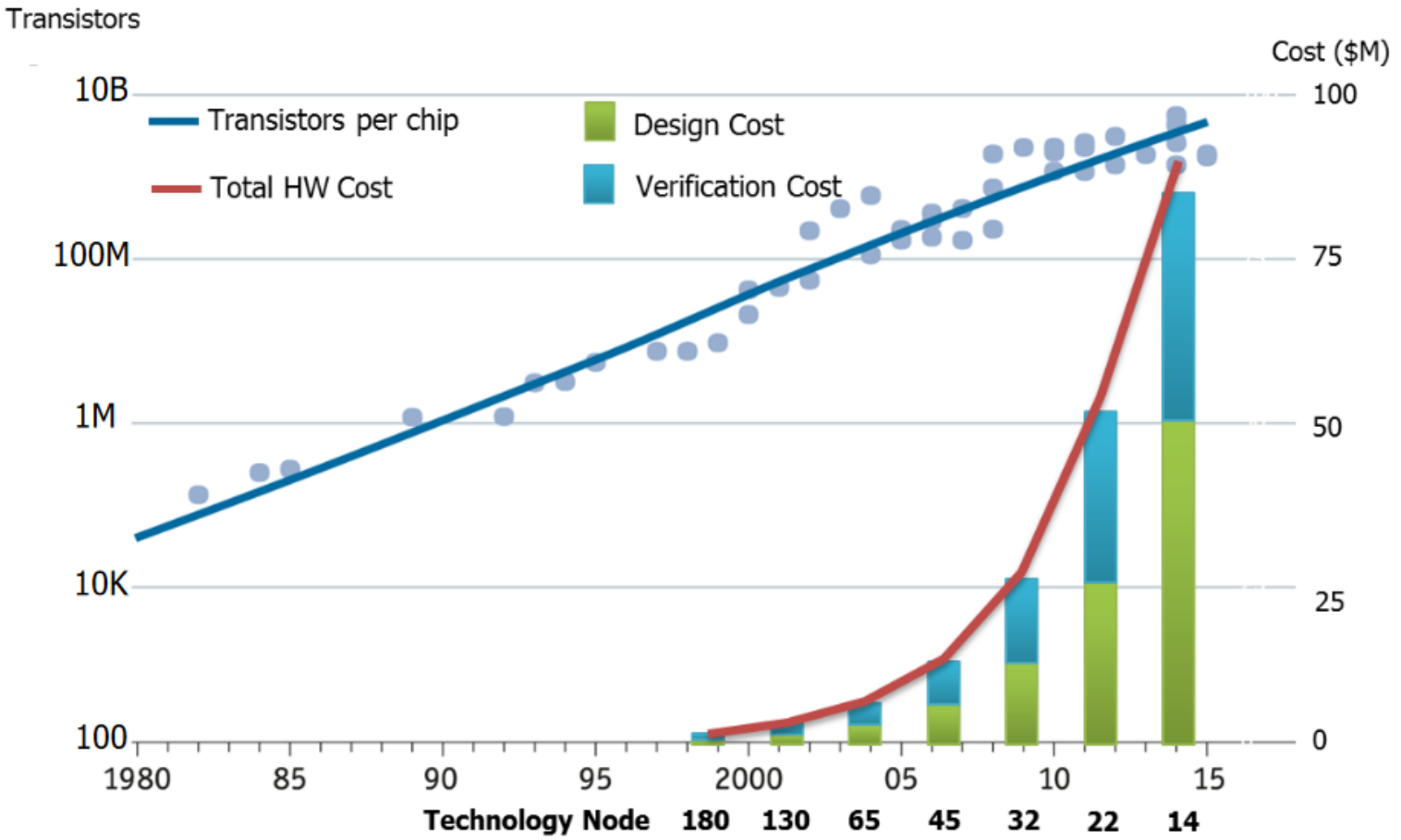
Report generator

OS (Linux) and shell scripting (bash, csh, tcl etc..)

Execution environment: X86, Virtual machine, remote servers, network resources

- **Development/programming**
  - Design: VHDL, SystemVerilog
  - Verification: Scripting, C, SystemVerilog, UVM
- **Debug**
  - Design, tool infrastructure knowledge
  - Communication and collaboration
- **Data management**
  - Running the tool flow with multiple set of input data
- **Maintenance the infrastructure**
- **Development of the infrastructure to increase automation**
- **Communication skills**

The costs: The typical plot



Olofsson, Andreas. "Silicon compilers-version 2.0." *keynote, Proc. ISPD* (2018).

- Cost function is exponential
  - Increase in technology complexity
  - Increase in design & project complexity
- The figure is illustrative and communicates the cost trend rather that plot of validated data.
- However, these plots doesn't tell how much select technology gets cheaper during the time
- Also design and verification costs can decrease during lifetime of the organizations and product platforms

The measures of the costs

Main cost of starting production
- Seems to be “list price”
- There are several ways to optimize this costs

Unit cost
Costs per wafer / # non-faulty chips on wafer
+ testing cost / chip
+ packaging cost/chip

Tech	250nm	180nm	130nm	90nm	65nm	40nm	28nm	16nm
Mask cost ($)	65K	105K	290K	560K	700K	1.25M	2.25M	5.70M
Cost per wafer ($)	720	790	2,950	3,200	3,300	4,850	7,600	11,100
Wafer diameter (mm)	200	200	300	300	300	300	300	300
Backend labor cost per gate ($) [30]	0.127	0.127	0.127	0.127	0.127	0.129	0.131	0.263

Table 1: **Wafer and mask costs rise exponentially with process node.** Backend cost per gate jumps with double-patterning.

Overview. Figure 1 examines the different metrics, based on data we collected from four sources in order of preference: 1) using CAD tools in our lab, 2) via Internet disclosures of technical data 3) by interviewing industry experts, and 4) using CMOS scaling to interpolate missing points. Recall that in CMOS scaling, the factor S refers to the ratio of

Tech Node (nm)	250	180	130	90	65	40	28	16
DRAM Ctlr	NA	NA	125	125	125	125	125	125
DRAM PHY	NA	NA	150	165	175	280	390	750
PCI-E Ctlr	NA	NA	90	90	125	125	125	125
PCI-E PHY	NA	NA	160	180	325	375	510	775
PLL	15	15	15	20	30	50	35	50
LVDS IO	7.5	7.5	0	150	90	36	40	200
Standard Cells, SRAM	0	0	0	0	0	100	100	100

Table 4: **IP Licensing Costs increase with advancing Technology Nodes.** Commonly used IP licensing costs across tech nodes, in late 2016, thousands of USD. Costs generally rise with node, but there are some irregularities.

Frontend Labor Salary [19]	$/yr	115K
Frontend CAD Licenses	$/Mm	4K
Backend Labor Salary [19]	$/yr	95K
Backend CAD Licenses	$/month	20K
Overhead on Salary		65%
Top-level gates		15K
NRE, flip-chip BGA package	$	105K

Table 3: **Node-independent NRE parameters in San Diego, CA in late 2016.** Mm=man-month. Backend Tools are more expensive than the people using them. Flip-chip packages add significant NRE.

- You do not always need latest technology
- During product lifetime costs are decreasing
- Product lifetime gives rooms for price optimizations e.g. test optimization
- For mass volume costs testing can be significant portion of the unit cost
- The SoC-hub consortium gains on having firsthand knowledge about the economical feasibility of SoC based solutions through chip design and prototyping activities

Khazraee, Moein, et al. "Moonwalk: Nre optimization in asic clouds." *ACM SIGARCH Computer Architecture News* 45.1 (2017)

SoC HUB *Example calculation with enhanced model*

- Salaries scaled from Silicon Valley to EU
- Technology costs scaled (2016 -> 2021)
- Calculations are for 28nm
- Scaling factors are rough based on visibility we have
- SoC-hub is constructing more detailed model for consortium internal usage
- All EDA tools abstracted to single average value.
  - Backend tools are expensive, but small number of licenses needed
  - Simulation tools are less expensive, but many of them needed
  - Pricing varies a lot based on many parameters
- IPs for fast interfaces are expensive

Remarks

- Around 1,4M (IoT node) & 0,9M (IoT edge) units production costs exceeds R&D costs
- Putting this to industry business perspective
  - Industry devices have high product price and cross margin compared to consumer products
  - Additional value created by SoC as differentiator to boost above
  - ***There are feasible business cases even with moderate volumes***

Input data	IoT Node	IoT Edge	
Duration of the project	1	1	years
Amount of D & V engineers	7	15	persons
Amount of backend engineers	2	3	persons
Design area	10	25	mm2
Num of 100mm2 chips on wafer	640	640	#
Num of designs on wafer	6400	2560	#
Yield	90 %	90 %	%.
Testing per chip	0,25	0,625	$
Packaging per chip	0,25	0,625	$

	IoT Node	IoT Edge	
Salaries	675	1350	k$
Tools in average	135	270	k$
Design Ips	26,25	412,5	k$
Technology	75	75	k$
R&D salaries, tools & technology	911250	2107500	$
Start of production	1125000	1125000	$
Total	2036250	3232500	$
Unit price (fabrication, testing and packaging)	1,489583	3,723958	$/unit

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Thank you!

Questions and feedback welcome! You can also contact later for further discussions

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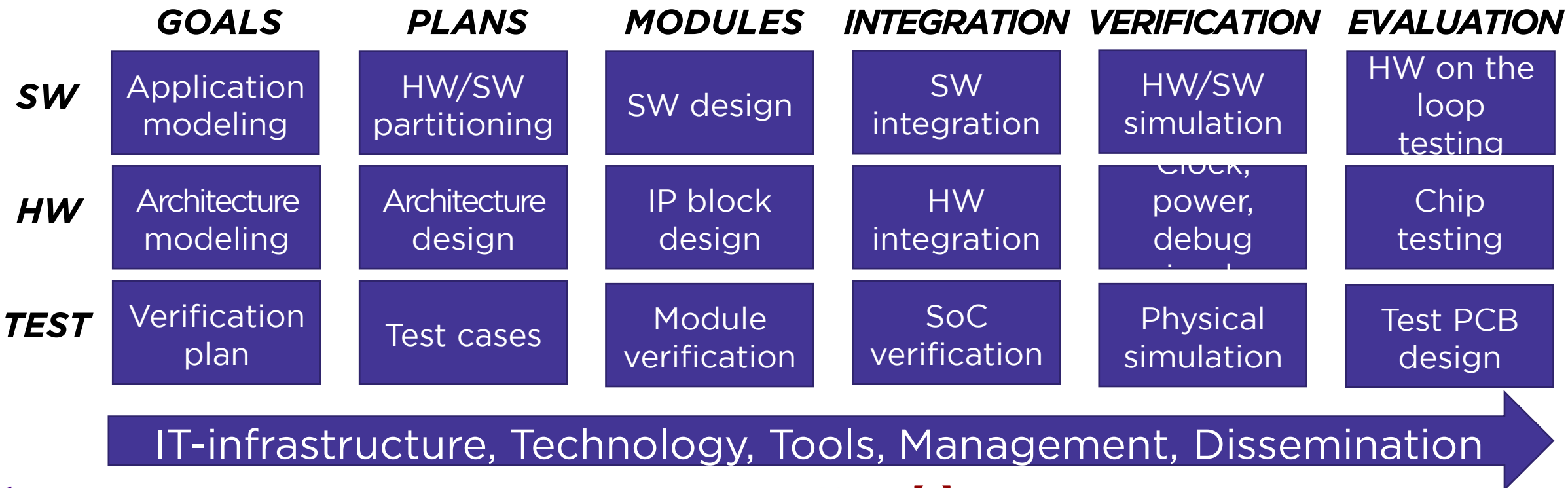
Closing Words

Timo Hämäläinen

SoC Hub is hiring – TAU and core partner companies

- If you are interested in joining SoC Hub team, please send to Suvi Lammi your
  - CV
  - Study record
  - Freeform motivation letter and what kind of tasks you are interested in



SoC Hub is hiring - TAU

Tampereen yliopisto
Tampere University

Back to the job list

Want to update your application?
Log in.

Postdoctoral Research Fellow (System-on-Chip design and implementation) / Tutkijatohtori (järjestelmäpiirien suunnittelu ja toteutus)

https://tuni.rekrytointi.com/paikat/?o=A_RJ&jgid=1&jid=882

SoC HUB *Your SoC?*

- Want to go further with your own idea on SoC? We offer
  1. Quick evaluation of the SoC feasibility
  2. Help finding partners
  3. Evaluation of SoC hub proto chips and template at your use case
  4. New co-development project
- How to start:
  - Contact SoC Hub at sochub@tuni.fi
  - Become Special Interest Group member
    - Share your needs with others
  - Free 2h early consultancy service
    - part of SoC Hub Tampere regional development project
    - company participants must fulfill De Minimis funding requirements

Next SoC Hub events

Hackathon
- RISC-V synthesis on FPGA
- SW toolchain setup
- RISC-V Linux build & boot
- RUST libraries

SoC design tools
- Cloud based tools
- Hands on

Workshops/webinars, Hackathons, SoC Hub coffee

SoC Hub Sprints

SoC prototype 1

SoC prototype 2

SoC prototype 3

SoC Hub expertise

SoC Hub architecture template & IPs & methodology

2021 2022 2023 2024

Contact information

@sochubfi

www.sochub.fi

sochub@tuni.fi

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Thank you!